

SYSTEM AND METHOD FOR EFFICIENTLY IMPLEMENTING A BATTERY CONTROLLER FOR AN ELECTRONIC DEVICE

BACKGROUND SECTION

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1. Field of the Invention

This invention relates generally to techniques for managing operating power of electronic devices, and relates more particularly to a system and
10 method for effectively implementing a battery controller for an electronic device.

2. Description of the Background Art

15 Implementing efficient methods for managing operating power is a significant consideration for designers and manufacturers of contemporary electronic devices. However, effectively managing operating power for electronic devices may create substantial challenges for system designers. For example, enhanced demands for increased power management
20 functionality and performance may require more system processing power and require additional hardware resources. An increase in processing or hardware requirements may also result in a corresponding detrimental economic impact due to increased production costs and operational inefficiencies.

25 Furthermore, enhanced system capability to perform various advanced power management operations may provide additional benefits to a system user, but may also place increased demands on the control and management of various system components. For example, an enhanced power management system that effectively monitors currently remaining operating
30 power for an electronic device may benefit from an effective implementation because of the importance of accurately indicating the currently-remaining available operating time for electronic device to a device user.

In certain operational environments that involve portable electronics devices, knowing in advance when a given battery pack will become fully-discharged is an issue of some importance to a device user. For example, when using a digital camera device to capture image data, failure to provide
5 sufficient operating power to the digital camera device may temporarily prevent capture of additional image data at a critical point in time.

Due to growing demands on system resources and the importance of successfully and accurately providing sufficient operating power to electronic devices, it is apparent that developing new techniques for managing operating
10 power is a matter of concern for related electronic technologies. Therefore, for all the foregoing reasons, developing efficient systems for managing operating power remains a significant consideration for designers, manufacturers, and users of contemporary electronic devices.

SUMMARY

In accordance with the present invention, a system and method for effectively implementing a battery controller for an electronic device are disclosed. In one embodiment, the battery controller may be implemented as a single-chip integrated circuit device that controls various functionalities of a battery pack for effectively providing operating power to the electronic device. In accordance with certain embodiments of the present invention, the battery controller may be selectively configured to control the battery pack in either a single-cell implementation or a dual-cell implementation.

In a single-cell implementation in which the battery pack provides a reduced battery supply voltage, the battery controller may utilize a charge pump to convert the battery supply voltage into a sufficient internal controller power supply for operating the battery controller. The battery controller may thus effectively utilize the foregoing charge pump to compensate for the reduced battery supply voltage resulting from a single-cell implementation of the battery pack.

Under certain conditions, the battery controller may open a discharge switch to prevent overdischarging the battery pack. In addition, the battery controller may also open a charge switch to prevent overcharging the battery pack under other conditions. In certain embodiments, the battery controller may utilize an internal negative charge pump to provide a negative charge-pump output voltage for generating an enhancement voltage so that the charge switch and the discharge switch may exhibit sufficiently low on-state resistances when turned on.

Certain embodiments of the battery controller may also include a UART device to perform various bi-directional communications between the battery controller and appropriate external entities such as a processor of the corresponding electronic device. The UART device may be advantageously implemented to communicate with the electronic device via a single transmit/receive pin on the integrated circuit device that contains the battery controller. In addition, the UART device may advantageously receive a

timebase signal from a precision on-chip instruction oscillator of the battery controller for accurately generating a UART clock signal to synchronize operations in the UART device. For at least the foregoing reasons, the present invention thus provides an improved system and method for

5 effectively implementing a battery controller for an electronic device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram for one embodiment of an electronic system,
in accordance with the present invention;

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FIG. 2 is a block diagram for one embodiment of the electronic device of
FIG. 1, in accordance with the present invention;

FIG. 3 is a block diagram for one embodiment of the battery controller
10 of FIG. 1, in accordance with the present invention;

FIG. 4 is a schematic diagram of selected components from one
embodiment of the battery pack of FIG. 1;

15 FIG. 5 is a schematic diagram of selected components from one
embodiment of the battery pack of FIG. 1, in accordance with the present
invention;

FIG. 6 is a schematic diagram of selected components from one
20 embodiment of the battery pack of FIG. 1, in accordance with the present
invention; and

FIG. 7 is a schematic diagram of selected components from one
embodiment of the UART of FIG. 3, in accordance with the present invention;
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DETAILED DESCRIPTION

The present invention relates to an improvement in power management techniques. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention comprises a system and method for effectively managing operating power for an electronic device, and may include a battery pack coupled to the electronic device for supplying operating power to the electronic device. A battery controller may be configured as a single integrated-circuit device to alternately manage the battery pack either in a single-cell implementation or in a dual-cell implementation. The battery controller may advantageously include a charge pump device to provide an internal controller power supply for operating the battery controller in the foregoing single-cell implementation.

Referring now to FIG. 1, a block diagram for one embodiment of an electronic system 110 is shown, in accordance with the present invention. In the FIG. 1 embodiment, electronic system 110 may include, but is not limited to, an electronic device 114, a battery pack 118, a battery charger 122, and a battery controller 310. In alternate embodiments, electronic system 110 may readily include various other components in addition to, or instead of, those components discussed in conjunction with the FIG. 1 embodiment.

In the FIG. 1 embodiment, electronic device 114 may be connected to battery pack 118 through a positive path and a negative path to receive

operating power. Battery controller 310 may perform various power management functions with regard to battery pack 118, and may also perform bi-directional communication procedures with electronic device 114 through a transmit/receive (TXRX) path. In the FIG. 1 embodiment, a
5 battery (one or more battery cells) in battery pack 118 may be connected to battery charger 122 through a positive charge path and a negative charge path for recharging the battery cell(s) in battery pack 118. The operation and utilization of electronic system 110 is further discussed below in conjunction with FIGS. 2-7.

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Referring now to FIG. 2, a block diagram for one embodiment of the FIG. 1 electronic device 114 is shown, in accordance with the present invention. For purposes of illustration, the FIG. 2 electronic device 114 is shown as being implemented as a digital camera device. However, in
15 alternate embodiments, electronic device 114 may readily be implemented as any other appropriate type of portable or stationary electronic device or system that requires operating power.

In the FIG. 2 embodiment, electronic device 114 includes, but is not limited to, a capture subsystem 222 and a device control module 218. In
20 alternate embodiments, electronic device 114 may readily include various other components in addition to, or instead of, those components discussed in conjunction with the FIG. 2 embodiment.

In the FIG. 2 embodiment, electronic device 114 may utilize capture subsystem 222 to selectively capture image data corresponding to a target
25 object via reflected light impacting an image sensor along an optical path. The foregoing image sensor, which may preferably include a charged-coupled device (CCD), may responsively generate a set of image data representing the target object. The image data may then be routed over device bus 238 to device control module 218 for appropriate processing
30 and storage.

In the FIG. 2 embodiment, device control module 218 may include, but is not limited to, a processor 226, a memory 230, and one or more

input/output interface(s) (I/O) 234. Processor 226, memory 230, and I/O 234 may each be coupled to, and communicate, via common device bus 238 that also communicates with capture subsystem 222. In the FIG. 2 embodiment, processor 226 may preferably be implemented to include any
5 appropriate microprocessor device for controlling electronic device 114.

Memory 230 may preferably be implemented as one or more appropriate storage devices, including, but not limited to, read-only memory, random-access memory, and various types of non-volatile memory, such as floppy disc devices, hard disc devices, or flash memory. I/O 234 preferably
10 may provide one or more effective interfaces for facilitating bi-directional communications between electronic device 114 and any external entity, including a system user or another electronic device.

In the FIG. 2 embodiment, memory 230 may include, but is not limited to, a camera application of program instructions that may be executed by
15 processor 226 to perform various functions and operations for electronic device 114. Memory 230 may also include a camera operating system that preferably controls and coordinates low-level functionality of electronic device 114.

Referring now to FIG. 3, a block diagram for one embodiment of the FIG. 1 battery controller 310 is shown, in accordance with the present invention. In alternate embodiments of the present invention, battery controller 310 may readily be implemented to include various other configurations, and may also include various elements and components in
20 addition to, or instead of, those discussed in conjunction with the FIG. 3 embodiment.

In the FIG. 3 embodiment, battery controller 310 may be implemented as a single-chip integrated circuit device that is integral with battery pack 118 (FIG. 1). In the FIG. 3 embodiment, battery controller 310 may include a
30 central processing unit (CPU) 314 which may be implemented to include any appropriate type of microprocessor device for controlling the functionality of battery controller 310. For example, CPU 314 may be effectively implemented

as a reduced-instruction-set computer (RISC) processor that executes battery controller instructions from program memory 318 to control the operation of battery controller 310.

In the FIG. 3 embodiment, battery controller 310 may also include, but
5 is not limited to, an analog-to-digital converter (ADC) module 322, a fuel gauge module 326, a universal asynchronous receiver/transmitter (UART) 334, linear blocks 336, an instruction oscillator 338, and a charge pump 342. In the FIG. 3 embodiment, battery controller 310 may utilize ADC module 322 to monitor battery voltage from one or more battery cells of
10 battery pack 118 (FIG. 1). CPU 314 may then utilize the foregoing measured battery voltage as one input value in a battery capacity algorithm for calculating currently-remaining operating power in battery pack 118. Similarly, battery controller 310 may utilize fuel gauge module 326 to monitor electrical current going into and out of the battery cell(s) of battery
15 pack 118 for use as another input value for the foregoing battery capacity algorithm.

In the FIG. 3 embodiment, battery controller 310 may utilize UART 334 and instruction oscillator 338 to perform various bi-directional communications between battery controller 310 and appropriate external
20 entities, as further discussed below in conjunction with FIG. 7. In the FIG. 3 embodiment, battery controller 310 may utilize linear blocks 336 (linear voltage regulators) and charge pump 342 to provide an internal controller power supply for operating various analog and digital circuits of battery controller 310. The implementation and utilization of linear blocks 336 and
25 charge pump 342 are further discussed below in conjunction with FIGS. 4-5.

Referring now to FIG. 4, a schematic diagram of selected components from one embodiment of FIG. 1 battery pack 118 is shown. In alternate embodiments, battery pack 118 may readily include various components and
30 configurations in addition to, or instead of, those discussed in conjunction with the FIG. 4 embodiment.

In the FIG. 4 embodiment, battery pack 118 may include battery controller 310 (FIG. 1) and a battery 454 which may be implemented by utilizing two battery cells. In certain embodiments, the foregoing battery cells may be implemented as lithium-ion battery cells that each supply
5 approximately 4.2 Volts to produce a total voltage of approximately 8.4 Volts when fully-charged.

In the FIG. 4 embodiment, battery pack 118 may also include a charge switch 422 and a discharge switch 458 that are connected in a series configuration in the positive charge path of battery pack 118, with charge
10 switch 422 being connected directly to a positive charger terminal (PCKP) 414, and with discharge switch 458 being connected to the positive side of battery 454. In the FIG. 4 embodiment, both charge switch 422 and discharge switch 458 may be implemented as P-channel field-effect transistors (FETs). In addition, in the FIG. 4 embodiment, charge switch 422
15 may be connected in parallel with a body diode 426, and discharge switch 458 may be connected in parallel with a body diode 462.

In operation, battery controller 310 may advantageously open discharge switch 458 to prevent overdischarging battery 454 below a minimum voltage level to thereby avoid permanently damaging battery 454.
20 In addition, battery controller 310 may also open charge switch 426 to prevent overcharging battery 454 above a maximum voltage level to thereby avoid certain hazardous conditions that may result from such overcharging of battery 454.

In certain other embodiments, charge switch 422 and discharge switch
25 458 may alternately be implemented by utilizing N-channel field-effect transistors (FETs) that are connected in a series configuration in the negative charge path of battery pack 118, with charge switch 422 being connected directly to negative charger terminal (PCKN) 418, and with discharge switch 458 being connected to the negative side of battery 454.

30 In the FIG. 4 embodiment, battery controller 310 may advantageously coordinate a startup procedure and a shutdown procedure for battery pack 118. In practice, when battery 454 is in a discharged state, a device user

may connect battery charger 122 (FIG. 1) to PCKP 414 and PCKN 418 to thereby initiate the foregoing startup procedure. Battery controller 310 may utilize the charger voltage at PCKP 414 to turn on charge switch 422 which then passes the charger voltage through LDOI pin 438 to the input of charger
5 regulator (LDOI LDO) 442.

Charger regulator 442 may thus output a regulated internal controller power supply 446 so that CPU 314 may begin executing battery controller instructions to control the operation of battery pack 118. In addition, CPU 314 may turn on discharge switch 458 to allow discharging battery 454. In
10 the FIG. 4 embodiment, CPU 314 may further utilize a BATTON line 450 to switch from charger regulator 442 to a battery regulator (BATT LDO) 474 which may then regulate battery voltage from BATT pin 470 to thereby provide the regulated internal controller power supply 446 for operating battery controller 310.

After battery 454 has been charged, battery pack 122 may be
15 disconnected for more unrestricted use of electronic device 114 (FIG. 1), and electronic device 114 may then utilize battery 454 for operating power. CPU 314 may utilize ADC module 322 (FIG. 3) of battery controller 310 to monitor battery 454 as it discharges. When a pre-determined discharged voltage level
20 is reached in battery 454, CPU 314 may responsively initiate a shutdown procedure for battery pack 118. For example, CPU 314 may open discharge switch 462, and may also toggle BATTON line 450 to switch battery controller 310 back to charger regulator 442 for the internal controller power supply 446. If battery charger 122 is not connected to battery pack 118, then the
25 internal controller power supply 446 of battery controller 310 will descend below a reset threshold, and battery pack 118 will enter a shutdown state until battery charger 122 is connected, and the previously-described startup procedure may be repeated.

In certain embodiments, it may be desirable or advantageous to
30 implement battery 454 by utilizing a single battery cell. Such a single-cell implementation, however, would provide only half the amount of battery voltage to drive battery regulator 474, which would therefore result in a

corresponding significant voltage reduction in the internal controller power supply 446 of battery controller 310. The analog and digital components of battery pack 118 may thus lack the required operating voltage to function properly. One embodiment for an effective single-cell implementation of
5 battery pack 118 is discussed below in conjunction with FIG. 5.

Referring now to FIG. 5, a schematic diagram of selected components from one embodiment of FIG. 1 battery pack 118 is shown, in accordance with the present invention. In alternate embodiments, the present invention
10 may readily utilize include various components and configurations in addition to, or instead of, those discussed in conjunction with the FIG. 5 embodiment.

In the FIG. 5 embodiment, battery pack 118 may include battery controller 310 (FIG. 1) and a battery 454 which may be implemented by
15 utilizing a single battery cell. A single-cell implementation of battery 454 may be selected for various factors, such as lower manufacturing costs and reduced size and weight of battery pack 118. In certain embodiments, the foregoing battery cell may be implemented as a lithium-ion battery cell that supplies approximately 4.2 Volts when fully-charged.

20 In the FIG. 5 embodiment, battery pack 118 may also include a charge switch 422 and a discharge switch 458 that are connected in a series configuration in the positive charge path of battery pack 118, with charge switch 422 being connected directly to a positive charger terminal (PCKP) 414, and with discharge switch 458 being connected to the positive side of
25 battery 454. In the FIG. 5 embodiment, both charge switch 422 and discharge switch 458 may be implemented as P-channel field-effect transistors (FETs). In addition, in the FIG. 5 embodiment, charge switch 422 may be connected in parallel with a body diode 426, and discharge switch 458 may be connected in parallel with a body diode 462.

30 In operation, battery controller 310 may advantageously open discharge switch 458 to prevent overdischarging battery 454 below a minimum voltage level to thereby avoid permanently damaging battery 454.

In addition, battery controller 310 may also open charge switch 426 to prevent overcharging battery 454 above a maximum voltage level to thereby avoid certain hazardous conditions that may result from such overcharging of battery 454.

5 In certain other embodiments, charge switch 422 and discharge switch 458 may alternately be implemented by utilizing N-channel field-effect transistors (FETs) that may be connected in a series configuration in the negative charge path of battery pack 118, with charge switch 422 being connected directly to negative charger terminal (PCKN) 418, and with
10 discharge switch 458 being connected to the negative side of battery 454.

 In the FIG. 5 embodiment, battery controller 310 may advantageously coordinate a startup procedure and a shutdown procedure for battery pack 118. In practice, when battery 454 is in a discharged state, a device user may connect battery charger 122 (FIG. 1) to PCKP 414 and PCKN 418 to
15 thereby initiate the foregoing startup procedure. Battery controller 310 may utilize the charger voltage at PCKP 414 to turn on charge switch 422 which then passes charger voltage through CPI0 pin 518 to a charger input (IN0) of charge pump 342.

 In accordance with the present invention, battery controller 310 may
20 utilize charge pump 342 to advantageously regulate voltage levels received at either of two selectable charge pump inputs to produce a desired charge pump output voltage by utilizing any appropriate means. In the FIG. 5 embodiment, charge pump 342 may operate in either a 1X mode, a 1.5 mode, or a 2X mode, depending upon how low the charge pump input voltage is
25 with respect to the desired charge pump output voltage. In 1X mode, the charge pump output voltage may be approximately equal to the charge pump input voltage. In 1.5X mode, the charge pump output voltage may be approximately 1.5 times the charge pump input voltage, and in 2X mode, the charge pump output voltage may be approximately twice the charge pump
30 input voltage. These foregoing selectable charge pump modes may be controlled by dedicated voltage comparators on the CPI0 and CPI1 inputs of charge pump 342 to thereby conserve unnecessary current consumption

caused by providing unnecessarily high operating voltages to battery controller 310.

In the FIG. 5 embodiment, charge pump 342 may pass the charge pump output voltage through CPO pin 526 and LDOI pin 438 to the input of charger regulator (LDOI LDO) 442. In the FIG. 5 embodiment, the foregoing charge pump output voltage may be approximately 4 Volts. Charger regulator 442 may then filter the charge pump output voltage to provide a clean and regulated internal controller power supply 446 so that CPU 314 may begin executing battery controller instructions to control the operation of battery pack 118.

In addition, CPU 314 may turn on discharge switch 458 to allow discharging battery 454. In the FIG. 5 embodiment, CPU 314 may further utilize a CPSEL line 530 to switch from the charger input (IN0) of charge pump 342 to a battery input (IN1) of charge pump 342. Charge pump 342 may then regulate battery voltage received from CPI1 pin 522 to thereby generate the charge pump output voltage at CPO pin 526. In the FIG. 5 embodiment, the charge pump output voltage at CPO pin 526 may be approximately 4 Volts. Battery controller 310 may thus effectively utilize charge pump 342 to compensate for the lower battery voltage resulting from the single-cell implementation of battery 454. As discussed above, charger regulator 442 may then utilize the charge pump output voltage to generate internal controller power supply 446 for operating battery controller 310.

In the FIG. 5 embodiment, CPU 314 may maintain BATTON line 450 at a value that permanently selects charge regulator 442 for providing internal controller power supply 446. In the single-cell implementation of FIG. 5, battery regulator 474 is typically not utilized. However, the FIG. 5 battery controller 310 may advantageously be implemented as a single integrated circuit device to include battery regulator 474 and other associated components necessary to utilize battery controller 310 in either the dual-cell implementation of battery pack 118 that was discussed above in conjunction with FIG. 4, or in the single-cell implementation discussed here in conjunction with FIG. 5. In the FIG. 5 embodiment, selection of either single-

cell mode or dual-cell mode for battery controller 310 may be determined by how connection pins from the integrated circuit device of battery controller 310 are connected.

In the FIG. 5 embodiment, after battery 454 has been charged, battery
5 pack 122 may be disconnected for more unrestricted use of electronic device 114 (FIG. 1), and electronic device 114 may then utilize battery 454 for operating power. CPU 314 may utilize ADC module 322 (FIG. 3) of battery controller 310 to monitor battery 454 as it discharges. When a pre-determined discharged voltage level is reached in battery 454, CPU 314 may
10 initiate a shutdown procedure for battery pack 118.

For example, CPU 314 may open discharge switch 462, and may also toggle CPSEL line 530 to switch battery controller 310 back to the charger input (IN0) of charge pump 342 for utilizing charger voltage from battery
15 charger 122 to generate the internal controller power supply 446. If battery charger 122 is not connected to battery pack 118, then the internal controller power supply 446 of battery controller 310 will descend below a reset threshold, and battery pack 118 will enter a shutdown state until battery charger 122 is connected, and the previously described startup procedure may be repeated.

20 In accordance with the present invention, charge pump 342 and the other circuitry of battery controller 310 may be implemented to prevent any leakage current to be drawn from battery 454 in shutdown mode. Furthermore, opening discharge switch 458 effectively disconnects battery from positive charger terminal (PCKP) 414 to eliminate any current leakage
25 through the charge path. Battery pack 118 may thus draw zero microamps of shutdown current from battery 454 during shutdown mode.

For purposes of illustration, the FIG. 4 and FIG. 5 embodiments are discussed above in the context of a single-cell implementation and a dual-cell implementation. However, the principles and concepts of the present
30 invention may readily be applied to battery controllers of any battery pack design that may be operated in environments in which a reduced-cell implementation and an increased-cell implementation of a particular battery

pack may result in variable amounts of battery supply voltage for operating the battery controller. For at least the foregoing reasons, the present invention thus provides an improved system and method for effectively implementing a battery controller 310 for an electronic device 114.

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Referring now to FIG. 6, a schematic diagram of selected components from one embodiment of FIG. 1 battery pack 118 is shown, in accordance with the present invention. In alternate embodiments, the present invention may readily utilize various components and configurations in addition to, or
10 instead of, those discussed in conjunction with the FIG. 6 embodiment.

In certain embodiments of battery pack 118, battery controller 310 may provide an enhancement voltage to turn on charge switch 422 via CHG pin 434. Similarly, battery controller 310 may provide an enhancement voltage to turn on discharge switch 458 via DIS pin 466. However, when battery 454
15 is implemented with a single battery cell as discussed above in conjunction with FIG. 5, then, even with the gates of charge switch 422 and discharge switch 458 pulled to a ground potential of zero Volts, there may not be sufficient enhancement voltage to completely turn on charge switch 422 and discharge switch 458.

20 In the FIG. 6 embodiment, battery controller 310 may utilize a charge amplifier 656 to provide the enhancement voltage for turning on charge switch 422 via CHG pin 434. Similarly, battery controller 310 may utilize a discharge amplifier 652 to provide the enhancement voltage for turning on discharge switch 458 via DIS pin 466. Charge amplifier 656 may receive a
25 positive voltage from battery charger 122 via PCKP pin 430, and discharge amplifier 652 may receive a positive voltage from battery 454 via BATT pin 470. In the FIG. 6 embodiment, the foregoing positive voltages may typically be as low as approximately 2 Volts for a fully-discharged battery cell.

30 Instead of connecting charge amplifier 656 and discharge amplifier 652 to ground, the FIG. 6 embodiment advantageously connects charge amplifier 656 and discharge amplifier 652 to a negative charge pump output 648 of an internal negative charge pump 614 in battery controller 310. In the FIG. 6

embodiment, internal negative charge pump 614 may provide a negative 2 Volts as the negative charge pump output 648. Charge amplifier 656 and discharge amplifier 652 may thus each generate a minimum of approximately 4 Volts of enhancement voltage so that charge switch 422 and discharge switch 458 may exhibit sufficiently low on-state resistances when turned on.

In the FIG. 6 embodiment, a phase 1 (PH1) switch 622 and a phase 1 (PH1) switch 628 may be closed to charge capacitor 618 with a charge pump output voltage from charge pump 342 (see FIG. 5) of battery controller 310 via CPO pin 526. Then, phase 1 switch 622 and phase 1 switch 628 may be opened, and a phase 0 (PH0) switch 636 and a phase 0 (PH0) switch 640 may be closed to provide the negative charge pump output 644 (NEG) from internal negative charge pump 614 to both charge amplifier 656 and discharge amplifier 652. In the FIG. 6 embodiment, CPU 314 of battery controller 310 may utilize NEGON line 660 to activate or deactivate internal negative charge pump 614.

As discussed above in conjunction with FIGS. 4 and 5, in certain embodiments, charge switch 422 and discharge switch 458 may alternately be implemented by utilizing N-channel field-effect transistors (FETs) that are connected in a series configuration in the negative charge path of battery pack 118, with charge switch 422 being connected directly to negative charger terminal (PCKN) 418, and with discharge switch 458 being connected to the negative side of battery 454. In an embodiment using N-channel field-effect transistors for charge switch 422 and discharge switch 458, battery controller 310 may not require the internal negative charge pump 614 discussed here in conjunction with FIG. 5 because battery controller 310 may advantageously utilize the charge pump output voltage of charge pump 342 (FIG. 5) on CPO pin 526 to generate sufficient enhancement voltage for completely turning on charge switch 422 and discharge switch 458.

Referring now to FIG. 7, a schematic diagram of selected components from one embodiment of FIG. 3 UART 334 is shown, in accordance with the present invention. In alternate embodiments, the present invention may

readily utilize include various components and configurations in addition to, or instead of, those discussed in conjunction with the FIG. 7 embodiment. In the FIG. 7 embodiment, battery controller 310 may utilize UART 334 to perform various bi-directional communications between battery controller
5 310 and appropriate external entities such as processor 226 of electronic device 114.

In the FIG. 7 embodiment, UART 334 may be advantageously implemented to communicate with electronic device 114 via a single transmit/receive (TXRX) pin on the integrated circuit device that contains
10 battery controller 310. This single-pin UART interface thus conserves available connection pins on the integrated circuit device of battery controller 310. In the FIG. 7 embodiment, electronic device 114 may transmit information via SO(TX) line 726 to the TXRX pin. UART 334 may then receive the transmitted information from the TXRX pin via RX line 14. Conversely,
15 UART 334 may transmit information via TX line 718 to the TXRX pin. Electronic device 114 may then received the transmitted information from the TXRX pin via SI(RX) line 722.

In the FIG. 7 embodiment, UART 334 may advantageously receive a timebase signal from instruction oscillator 338 (FIG. 3) of battery controller
20 310 for accurately generating a UART clock signal to synchronize operations in UART 334. Since the instruction oscillator 338 includes a precision timebase circuit that resides onboard the integrated circuit of battery controller 310, UART 334 therefore does not require an off-chip crystal oscillator to generate the foregoing timebase signal. In addition, extra
25 connection(s) to support such an off-chip timebase source are not required in the FIG. 7 implementation of UART 334.

The invention has been explained above with reference to certain embodiments. Other embodiments will be apparent to those skilled in the art
30 in light of this disclosure. For example, the present invention may readily be implemented using configurations and techniques other than those described in the embodiments above. Additionally, the present invention may

effectively be used in conjunction with systems other than those described above. Therefore, these and other variations upon the discussed embodiments are intended to be covered by the present invention, which is limited only by the appended claims.

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